In The Claims

1. (currently amended) A charge pump, comprising:

a voltage source for providing an input voltage;

a signal source for providing a clocking signal and a phase inverted signal of the clocking signal needed to operate the charge pump;

a first control signal generation unit, wherein the first control signal generation unit receives the input voltage, the phase inverted clocking signal and a ground voltage and outputs a first control signal, and the voltage level of the first control signal is determined by the phase inverted clocking signal;

a first output voltage generation unit, wherein the first output voltage generation unit receives the input voltage and the first control signal and outputs via a first output terminal, and where [[~~the~~]]a connection of the input voltage with the first output terminal is determined by a circuit inside the first output voltage generation unit that depends on the first control signal;

a second control signal generation unit, wherein the second control signal generation unit receives the input voltage, the clocking signal and [[~~a~~]]the ground voltage and outputs a second control signal, and the voltage level of the second control signal is determined by the clocking signal;

a second output voltage generation unit, wherein the second output voltage generation unit receives the input voltage and the second control signal and outputs via a second output terminal, and where [[~~the~~]]a connection of the input voltage with the second output terminal is determined by a circuit inside the second output voltage generation unit that depends on the second control signal;

a first capacitor having a first terminal receiving the clocking signal and a second

terminal to output a first output voltage, and the second terminal of the first capacitor is connected to the first output terminal; and

a second capacitor having a first terminal receiving the phase inverted clocking signal and [[~~the~~]]a second terminal to output a second output voltage, and the second terminal of the second capacitor is connected to the second output terminal.

2. (currently amended) The charge pump in claim 1, wherein [[~~a~~]]the first output voltage generation unit further comprising:

a first P-type metal oxide semiconductor (PMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the drain terminal of the first PMOS transistor is connected to the second terminal of the first capacitor and the substrate of the first PMOS transistor, and the source terminal of the first PMOS transistor is connected to the input voltage;

a second P-type metal oxide semiconductor (PMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the drain terminal of the second PMOS transistor is connected to the second terminal of the first capacitor and the substrate of the second PMOS transistor, the source terminal is connected to the gate terminal of the first PMOS transistor, and the gate terminal of the second PMOS transistor is connected to the input voltage, wherein the first and second PMOS's form a part of the circuit.

3. (currently amended) The charge pump in claim [[~~1~~]]2, wherein [[~~a~~]]the first control signal generation unit further comprising:

a first N-type metal oxide semiconductor (NMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the gate of the first NMOS transistor is connected to the input voltage, the source terminal of the first NMOS transistor is connected to the gate of the first PMOS transistor, and the substrate of the first NMOS transistor is connected to the ground;

a second N-type metal oxide semiconductor (NMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the drain terminal of the second NMOS transistor and the substrate of the second NMOS transistor are connected to the ground, the source terminal of the second NMOS transistor is connected to the drain terminal of the first NMOS transistor and the gate of the second NMOS transistor receives the phase inverted clocking signal.

4. (currently amended) The charge pump in claim 1, wherein [[a]]the second output voltage generation unit further comprising:

a [[~~third~~]]first P-type metal oxide semiconductor (PMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the drain terminal of the [[~~third~~]]first PMOS transistor is connected to the second terminal of the second capacitor and the substrate of the [[~~third~~]]first PMOS transistor, and source terminal of the [[~~third~~]]first PMOS transistor is connected to the input voltage;

a [[~~fourth~~]]second P-type metal oxide semiconductor (PMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the drain terminal of the [[~~fourth~~]]second PMOS transistor is connected to the second terminal of the second capacitor and the substrate of the [[~~fourth~~]]second PMOS transistor, the source terminal of the [[~~fourth~~]]second PMOS transistor is connected to the gate terminal of the [[~~third~~]]first PMOS transistor, and the gate terminal of the [[~~fourth~~]]second PMOS transistor is connected to the input voltage, wherein the first and second PMOS's form a part of the circuits.

5. (currently amended) The charge pump in claim [[~~1~~]]4, wherein [[a]]the second control signal generation unit further comprising:

a [[~~third~~]]first N-type metal oxide semiconductor (NMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the gate of the [[~~third~~]]first NMOS transistor is

connected to the input voltage, the source terminal of the [[~~third~~]]first NMOS transistor is connected to the gate of the [[~~third~~]]first PMOS transistor, and the substrate of the [[~~third~~]]first NMOS transistor is connected to the ground;

a [[~~fourth~~]]second N-type metal oxide semiconductor (NMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the drain terminal of the [[~~fourth~~]]second NMOS transistor and the substrate of the [[~~fourth~~]]second NMOS transistor are connected to the ground, the source terminal of the fourth NMOS transistor is connected to the drain terminal of the [[~~third~~]]first NMOS transistor and the gate of the fourth NMOS transistor receives the clocking signal.

6. (currently amended) A voltage doubler with a charge pump as in [[~~claim1~~]]claim 1 therein, further comprising

an output voltage switching unit receiving the first and second output [[~~voltage~~]]voltages, and delivering a final output voltage.

7. (currently amended) The voltage doubler of claim 6, wherein the output voltage switching unit comprising:

a fifth P-type metal oxide semiconductor (PMOS) transistor having a substrate, a gate, a drain a source terminal, wherein the source terminal of the fifth PMOS transistor receives the second output voltage, the drain terminal of the fifth PMOS transistor is connected to the substrate of the fifth PMOS transistor, and the gate of the fifth PMOS transistor receives the first output voltage;

a sixth P-type metal oxide semiconductor (PMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the source terminal of the sixth PMOS transistor receives the first output voltage, the drain terminal of the sixth PMOS transistor is connected to the

substrate of the sixth PMOS transistor, and the gate of the sixth PMOS transistor receives the second output voltage;

a seventh P-type metal oxide semiconductor (PMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the source terminal of the seventh PMOS transistor is receiving the second output voltage, the drain terminal of the seventh PMOS transistor connects to a final output voltage terminal, the substrate of the seventh PMOS transistor is connected to the substrate of the fifth PMOS transistor, and the gate of the seventh PMOS transistor receives the first output voltage;

an eighth P-type metal oxide semiconductor (PMOS) transistor having a substrate, a gate, a drain and a source terminal, wherein the source terminal of the eighth PMOS transistor is receiving the first output voltage, the drain terminal of the eighth PMOS transistor is connected to the final output voltage terminal, the substrate of the eighth PMOS transistor is connected to the substrate of the sixth PMOS transistor, and the gate of the eighth PMOS transistor is receiving the second output voltage;

an output capacitor having two terminals, wherein one terminal is connected to the ground and the other terminal is connected to the final output voltage terminal; and

a substrate capacitor having two terminals, wherein one terminal is connected to the ground and the other terminal is connected to the substrate of the fifth PMOS transistor.